REMARKS

Claims 1-3 and 6 are pending and are rejected. Claim 1 has been amended, and claims 7-8 have been added. The applicant respectfully requests reconsideration in view of the amendment and remarks.

Applicant thanks the Examiner for the second telephone interview on April 21, 2008.

Section 103(a) Rejections

During the interview, the Examiner indicated that Claim 1 was confusing because the limitation of "transferring the second portion of the data packet ... to the registers" was placed after the limitation of "a second portion is stored in the registers." Claim 1 has been amended to address the Examiner's concerns.

In addition, claim 1 has been amended to require the plurality of registers are not included in the memory. Support may be found on page 6, lines 28-30 of the application.

Claims 1-3 and 6 stand rejected as obvious over U.S. Patent No. 5,289,470 ("Chang") in view of U.S. Patent No. 6,032,190 ("Bremer").

Chang teaches a networking device which, when a data packet is received, stores the data packet into a first packet buffer. If the size of the data packet is greater than the first buffer, then further data from the packet is stored into a second buffer. Although the second buffer can be a different size than the first buffer, "their respective sizes are in accordance with the predetermined ordered sequence of buffer sets" (column 5, lines 50-54). Once stored, the data then remains in the buffer to which it has been stored.

First, claim 1 recites "a control unit for determining whether the data packet to be stored in one of the queues meets a criterion for efficient storage in the packet buffers." Chang teaches using a predetermined ordered sequence of buffer sets of different sizes, not determining whether a data packet meets a criterion for efficient storage. The section of Chang indicated by the Examiner merely teaches the completely convention step of determining whether a buffer is full and a new buffer is needed, not whether a criterion for efficient storage has been met.

Second, claim 1 recites "the data switch is arranged to initially store a first portion of the data packet in a first packet buffer and store a second portion of the data packet in a second packet buffer so that the first packet buffer is full and the second packet buffer is only partially full", and "upon the control unit making a negative determination, transferring the second portion of the data packet from the second packet buffer to at least one of the registers so that the first portion is stored in the packet buffers and the second portion is stored in the registers." In Chang, all of the data is stored into and stays in the allocated buffer. Chang simply does not teach transferring a second portion of a data packet from a second packet buffer to at least one of the registers so that a first portion is stored in the packet buffers and the second portion is stored in the registers.

Figure 4 of Bremer shows that a header of a data packet is sent to registers 150 while the data is directed to a buffer 50. Bremer fails teach determining whether a data packet meets a criterion for efficient storage, or transferring a portion of the data packet from a packet buffer to at least one of the registers, much less transferring a portion of the data packet upon a negative determination of the a criterion for efficient storage. Thus, Bremer does not supply what Chang lacks.

Consequently, claim 1, and the claims depending therefrom, cannot be obvious over the combination of Chang and Bremer.

New claim 7 requires a first memory divided into packet buffers, a second memory for storing a threshold value, a plurality of registers that are not included in the first memory and second memory; and a control unit for determining whether a data packet to be stored in one of the queues meets a criterion for efficient storage in the packet buffers. In addition, on a negative determination of the criterion, at least a portion of the data packet is stored in one of the registers.

New claim 7 should be similarly allowable as claim 1. In particular, Chang teaches using a predetermined ordered sequence of buffer sets of different sizes, not determining whether a data packet meets a criterion for efficient storage. Moreover, Chang teaches storing all parts of the data packet in the buffer. Although Bremer teaches storing the header of a data packet in a register, it fails to teach storing any portion on a negative determination of a criterion for

efficient storage. Moreover, Bremer always stores the data portion of the packet into the data buffer. Bremer certainly does not teach storing the data packet in at least one of the registers if the size of the data packet is less than that of a packet buffer and the size of the data packet is below a threshold value.

A petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge the fee for the extension of time in the amount of $120 to Deposit Account 06-1050. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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